

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Brian S. Doyle, et al.

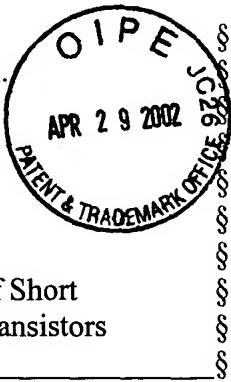
Serial No. 10/045,376

Group Art: Not Yet Assigned

Filed: November 9, 2001

Examiner: Not Yet Assigned

For: Methodology for Control of Short
Channel Effects in MOS Transistors



Commissioner of Patents
Washington, D.C. 20231

SUBMISSION OF INVENTION DISCLOSURE STATEMENT AND REFERENCES

Dear Sir:

The attached Invention Disclosure Statement and accompanying references are hereby submitted for consideration by the Examiner. These were previously submitted but were apparently never placed in the file. Attached is a photocopy of the return postcard showing that the IDS was previously received by you.

No fee is believed due with this submission. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOLOKOFF TAYLOR & ZAFMAN LLP

Date: 4-22-02

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Serial/Patent No. *Not Yet Assigned* Filing/Issue Date *11-9-01*
Client: *Intel Corporation* Atty/Secty Initials: *WWR/faw (REH)*
Title: *Methodology for Control of Short Channel Effects in MOS Transistor*
BSTZ File No. *42390P576812* Docket Due Date: _____
Date Mailed: *01-25-02*

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Other *14 cited JDS References* Serial # *10045376*

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		Application Number	10/045,376	
		Filing Date	11-09-2001	
		First Named Inventor	Brian S. Doyle, et al.	
		Group Art Unit	Not Yet Assigned	
		Examiner Name	Not Yet Assigned	
Total Number of Pages in This Submission		Attorney Docket Number		42390P5768D

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Date	4-22-02

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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T2
		G.A. HISHMEH & L. CARTZ, F. DESAGE, C. TEMPLIER, & J.C. DESOYER, R.C. BIRTCHER; Rare Gas Bubbles in Muscovite Mica Implanted with Xenon and Krypton; J. Mater. Res., Vol. 9 No. 12, December 1994, pp. 3095-3107.	
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		V. RAINERI, G. FALLICA, S. LIBERTINO; Lifetime Control in Silicon Devices by Voids Induced by He Ion Implantation; J. Appl. Phys. 79 (12), 15 June 1996, American Institute of Physics; pp. 9012-9016.	
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		J.W. MEDERNACH, T.A. HILL, S.M. MYERS, AND T.J. HEADLEY; Microstructural Properties of Helium Implanted Void Layers in Silicon as Related to Front-Side Gettering; J. Electrochem. Vol. 143, No. 2, February 1996, The Electrochemical Society, Inc., pp. 725-735.	

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